Hall Ticket Number:

Code No. : 31302

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (E.C.E.) III Year I-Semester (Main) Examinations, Nov./Dec.-2016

Digital Integrated Circuits and Applications

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Define propagation delay and noise margin of a digital IC.
2. Is direct interfacing of CMOS to TTL gates possible? Justify.
3. Interpret the effect on Noise margin and Power dissipation in CMOS IC with the increase in power supply (V_{DD}).
4. Define dynamic MOS logic. When is it preferred?
5. Design full subtractor circuit using two 4×1 line multiplexers.
6. Show that IC74138 can be used as a Decoder and a Demultiplexer.
7. Define set-up time and hold time for a flip-flop.
8. Draw the circuit diagram of a serial input-serial output shift register and mention standard ICs with this function.
9. Brief about PLA and how capacity of PLA is specified?
10. Design a RAM system of 1K×8 bit capacity using 512×8 bit RAM devices.

Part-B (5 × 10 = 50 Marks)

11. a) Write significance of open collector output of a TTL gate. What is its utility? Draw the circuit showing open collector output and pull-up resistor. [5]
    b) List various specifications of digital ICs. Give some typical values of each of them. [5]
12. a) Explain the working of two input ECL-OR/NOR gate with the help of a neat diagram. [6]
    b) Describe the operation of a CMOS transmission gate and give its applications. [4]
13. a) Construct a 5×32 line decoder with four 3×8 line decoders and one 2×4 line decoder. [5]
    b) Design a two-bit magnitude comparator with suitable gates. [5]
14. a) Design a mod-5 lock free synchronous counter using Master Slave JK flip-flops and draw timing diagram for a continuous clock. [5]
    b) Design a universal Shift register using D-flip flops. [5]
15. a) Implement a 3-bit binary to gray code converter using suitable PLD. [5]
    b) Distinguish between ROM and RAM. Explain DRAM cell with read, write and refresh control signals. [5]
16. a) Determine the maximum number of 7400 TTL NAND gate inputs that can be driven by a 7400 NAND gate TTL output. From the data sheet I_{OL} (max) = 16 mA; I_{IL} (max) = –1.6 mA; I_{OH} (max) = –400μA; I_{IH} (max) = 40 μA. [4]
    b) Describe the operation of four input CMOS NAND gate with a circuit diagram. [6]
17. Write short notes on any ***two*** of the following:
    a) Single Digit BCD adder [5]
    b) 7490 counter [5]
    c) PLA architecture. [5]

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